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James C. Scheller
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Seventh Floor
12400 Wilshire Boulevard
Los Angeles, CA 90025-1026

EXAMINER	
LI, AIMEE J	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 01/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/038,431	TRIVEDI ET AL.	
	Examiner	Art Unit	
	Aimee J. Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,9-18,20-32 and 34-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9-18,20-32 and 34-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-7, 9-18, 20-32, 34-39, and 40-41 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: Amendment as received on 26 October 2005.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claim 41 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 40 states "wherein the memory controller is usable by a central processing unit (CPU) not disposed on the integrated circuit to access the memory." Claim 23 states "wherein the microprocessor is a media processor disposed on an integrated circuit with a memory controller". The specification has not disclosed how a memory controller is not on the integrated circuit with a processor while the processor is on the integrated circuit with the memory controller.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-3, 5-7, 9-14, 16-18, 20-28, 30-32, 34-38, and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chehrazi et al., U.S. Patent No. 6,282,556 (herein referred to as Chehrazi) in view of Mennemeier et al., U.S. Patent No. 6,036,350 (herein referred to as Mennemeier).

7. Regarding claims 1, 12, 23 and 26, taking claim 1 as exemplary, Chehrazi has taught a method for execution by a microprocessor in response to receiving a single instruction (Chehrazi Col.20 lines 42-52), the method comprising:

a. Receiving a first plurality of numbers (Chehrazi 310 of Fig.20B, Col.20 line 62 – Col.21 line 1) and a second plurality of numbers (Chehrazi 312 of Fig.20B, Col.20 line 62 – Col.21 line 1),

b. Generating a third plurality of numbers, each of which is an absolute difference between a number in the first plurality of numbers and a number in the second plurality of numbers (Chehrazi Col.21 lines 6-12),

c. Wherein the sum of third plurality of numbers are saved in an entry in a register file (Chehrazi Col.20 lines 47-58),

d. Wherein the above operations are performed in response to the microprocessor receiving the single instruction (Chehrazi Col.20 lines 42-52, 61-62).

8. Chehrazi has not explicitly taught wherein the third plurality of numbers themselves are saved in an entry in a register file. However, Mennemeier has taught storing a third plurality of numbers, specifically a vector of absolute differences, in a instruction specified register (Mennemeier, Col.7 line 64 – Col.8 line 23) so that the absolute differences can be used in other

operations that require the distance assessment that the results represent (Mennemeier, Col.8 line 21-23). One of ordinary skill in the art would have recognized that it is desirable to retain results that will be used by future instructions so that the results don't need to be recalculated. Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Chehrazi to store the absolute differences, rather than the sum of the absolute differences, in an instruction specified register so that the values could be reused by other operations that require the data, thus improving throughput by avoiding the recalculation of the data.

9. Claims 12, 23, and 26 are nearly identical to claim 1. However, Chehrazi has taught the differences. Claim 12 differs in the claim being comprised within a machine-readable media (Chehrazi Col.20 lines 42-46), while claims 23 and 26 differs in the claims being comprised within an execution unit (Chehrazi Col.7 lines 20-40). Also, claim 23 claims wherein the microprocessor is a media processor disposed on an integrated circuit with a memory controller (Chehrazi column 5, lines 43-54). Besides these differences, the claims encompass the same scope as claim 1. Thus, claims 12, 23 and 26 are rejected for the same reasons as claim 1.

10. Regarding claims 2, 13, 24 and 27, taking claim 2 as exemplary, Chehrazi has taught a method as in claim 1, wherein an absolute difference between a first number and a second number is computed using a method comprising:

a. Producing a first intermediate number by subtracting the second number from the first number (Chehrazi Col.21 lines 1-8),

b. Producing a second intermediate number by subtracting the first number from the second number (Chehrazi Col.21 lines 1-8),

c. Selecting a positive number from the first intermediate number and the second intermediate number as the absolute difference between the first number and the second number (Chehrazi Col.21 lines 8-12),

d. Wherein the microprocessor is a media processor (Chehrazi 108 of Fig.1, Col.3 lines 6-7) disposed on an integrated circuit with a memory controller (Chehrazi 100 of Fig.1, Col.5 lines 46-54).

11. Claims 13, 24 and 27 are nearly identical to claim 2. Claim 13 lacks the recitation of a media processor disposed on an integrated circuit with a memory controller, and claims 13, 24 and 27 differ in their parent claims, but encompass the same scope as claim 2. Thus, claims 13, 24 and 27 are rejected for the same reasons as claim 2.

12. Regarding claims 3, 14 and 28, taking claim 3 as exemplary, Chehrazi has taught a method as in claim 2, wherein the first intermediate number and the second intermediate number are produced in parallel (Chehrazi Col.21 lines 1-8), and wherein the third plurality of numbers are generated substantially simultaneously (Chehrazi Col.21 lines 8-12).

13. Claims 14 and 28 are nearly identical to claim 3, both differing in their lack of having the third plurality of numbers being generated substantially simultaneously, as well as differing in their parent claims, but both encompass the same scope as claim 3. Thus, Claims 14 and 28 are rejected for the same reasons as claim 3.

14. Regarding claims 5, 16 and 30, taking claim 5 as exemplary, Chehrazi has taught a method as in claim 1, wherein the first plurality of numbers are received from a first entry in the register file (Chehrazi Col.20 lines 47-58).

15. Claims 16 and 30 are nearly identical to claim 5, differing in their parent claims, but encompassing the same scope as claim 5. Thus, claims 16 and 30 are rejected for the same reasons as claim 5.

16. Regarding claims 6, 17 and 31, taking claim 6 as exemplary, Chehrazi has taught a method as in claim 5, wherein the single instruction specifies a way to partition a string of bits in the first entry into a first plurality of numbers (Chehrazi Col.20 lines 61-65). Here, the SABD instruction specifies a register in the register file, which corresponds to the plurality of numbers, and specifies that the data in the register be interpreted to be 16 separate 8-bit numbers.

17. Claims 17 and 31 are nearly identical to claim 6, differing in their parent claims, but encompassing the same scope as claim 6. Thus, claims 17 and 31 are rejected for the same reasons as claim 6.

18. Regarding claims 7, 18 and 32, taking claim 7 as exemplary, Chehrazi has taught a method as in claim 5, wherein the single instruction specifies an index of the entry in the first register file (Chehrazi 560c and 560d of Fig.20a, Col.20 lines 47-58).

19. Claims 18 and 32 are nearly identical to claim 7, differing in their parent claims, but encompassing the same scope as claim 7. Thus, claims 18 and 32 are rejected for the same reasons as claim 7.

20. Regarding claims 9, 20 and 34, taking claim 9 as exemplary, Chehrazi in view of Mennemeier has taught a method as in claim 1, wherein the single instruction specifies an index of the entry in a the register file (Mennemeier, Col.7 line 64 – Col.8 line 23, as well as above paragraph 39).

21. Claims 20 and 34 are nearly identical to claim 9, differing in their parent claims, but encompassing the same scope as claim 9. Thus, claims 20 and 34 are rejected for the same reasons as claim 9.

22. Regarding claims 10, 21 and 35, taking claim 10 as exemplary, Chehrazi has taught a method as in claim 1, wherein a type of each of the first and second pluralities of numbers is one of:

a. Unsigned integer (Chehrazi Col.20 lines 54-55),

b. Signed integer (Chehrazi Col.20 lines 54-55),

c. Floating-point number.

23. Here, because the claim is written in the alternative format, only one of the three possible limitations is required to be met. Thus, Chehrazi has taught the limitations of claim 10.

24. Claims 21 and 35 are nearly identical to claim 10, differing in their parent claims, but encompassing the same scope as claim 10. Thus, claims 21 and 35 are rejected for the same reasons as claim 10.

25. Regarding claim 11, 22 and 36, taking claim 11 as exemplary, Chehrazi has taught a method as in claim 1, wherein a size of each of the first and second pluralities of numbers is one of:

a. 8 bits (Chehrazi Col.20 lines 61-65),

b. 16 bits,

c. 32 bits.

26. Here, because the claim is written in the alternative format, only one of the three possible limitations is required to be met. Thus, Chehrazi has taught the limitations of claim 11.

27. Claims 22 and 36 are nearly identical to claim 11, differing in their parent claims, but encompassing the same scope as claim 11. Thus, claims 22 and 36 are rejected for the same reasons as claim 11.

28. Regarding claim 25, Chehrazi has taught a processing system comprising an execution unit as in claim 23 (Chehrazi Fig.1).

29. Regardin claim 37, Chehrazi has taught wherein a type of each of the first and second pluralities of numbers is floating point number (Chehrazi column 1, lines 19-21 and column 9, lines 37-41).

30. Regarding claim 38, Chehrazi has taught wherein the microprocessor is a media processor disposed on an integrated circuit with a memory controller (Chehrazi column 5, lines 43-54).

31. Regarding claim 40, Chehrazi has taught wherein the memory controller is usable to access memory not disposed on the integrated circuit (Chehrazi Col. 5 lines 36-60 and Figure 1). As can be seen in Chehrazi's Figure 1, the ROM and RAM memories and data storage device are separate from the processor.

32. Claims 4, 15, 29, and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chehrazi et al., U.S. Patent No. 6,282,556 (herein referred to as Chehrazi) in view of Mennemeier et al., U.S. Patent No. 6,036,350 (herein referred to as Mennemeier) as applied to claims 1, 2, 12, 26, and 27 above, and further in view of Diefendorff et al., EPO 0 485 776 A2 (herein referred to as Diefendorff).

33. Regarding claims 4, 15, 29, and 39, taking claim 4 as exemplary, Chehrazi has taught taking an absolute difference between a first number and a second number (Chehrazi Col.21 lines 6-12). Chehrazi has not taught:

a. Testing if an overflow occurs in producing the first intermediate number and the second intermediate number,

b. Saturating the difference between the first number and the second number if an overflow occurs.

34. Diefendorff has taught

a. Testing if an overflow occurs in producing the first intermediate number and the second intermediate number (Diefendorff column 6, lines 42-46; column 11, lines 38-41; column 11, line 56 to column 12, line 12; and Figure 5),

b. Saturating the difference between the first number and the second number if an overflow occurs (Diefendorff column 6, lines 42-46; column 11, lines 38-41; column 11, line 56 to column 12, line 12; and Figure 5).

35. A person of ordinary skill in the art at the time the invention was made would have recognized, and as taught by Diefendorff, that overflow testing and saturation arithmetic improves the handling of overflow conditions during shading or image processing, thereby improving the quality of the image and accelerating the performance of the microprocessor during shading and image processing. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the overflow testing and saturation arithmetic of Diefendorff in the device of Chehrazi to improve image quality and accelerate the performance of a microprocessor during shading and image processing.

Response to Arguments

36. Applicant's arguments filed 26 October 2005 have been fully considered but they are not persuasive.

37. Applicant argues on pages 11-12, 13-14, and 15-17 in essence

> Although any evidence submitted to traverse the rejection or objection on a basis ***not otherwise provided for*** must be by way of an oath or declaration under this section, the evidence used for the argument has been ***otherwise provided for***. Specifically, the long felt need is established based upon the references and reasoning provided by the Examiner...
>
> Specifically, the references and at least some of the reasoning provided the Examiner to establish the obviousness are used to establish 'the long felt need', which contradicts the conclusion of obviousness. The Examiner relied upon the cited references to establish the need/motivation. If this reasoning of the Examiner were proper, the age of the references would further establish the element of 'long felt'. Thus, 'the long felt need' is based on the evidence already provided by the Examiner.

38. This has not been found persuasive. Merely relying on the dates and ages of references cited by the Examiner in a rejection does not establish long felt need nor does it imply long felt need. The basis for obviousness is what the two references would have suggested to a person of ordinary skill in the art, and, while there is a small basis of need in the reasoning, this does not establish a blatant long felt need, as suggested by Applicant's arguments. It says in 37 CFR 1.132

> When any claim of an application or a patent under reexamination is rejected or objected to, any ***evidence submitted to traverse the rejection*** or objection ***on a basis not otherwise provided*** for must be by way of an oath or declaration under this section.

39. The "long felt need" basis is a traversal ***not*** provided by the Examiner. As stated about, the mere dates and ages of the references provided are ***not*** a valid basis for a "long felt need" traversal. As is stated in the MPEP 716.04, to establish "long felt need" there must be "objective evidence that an art recognized problem existed in the art for a long period of time without solution." No objective evidence that that "an art recognized problem existed" has been presented, let along that the problem has existed "for a long period of time without solution." There is no evidence provided that there were attempts to solve the problem presented nor is there evidence that the attempts resulted in failure. As is stated in MPEP 716.04 I, there are several factors that must be met in order to meet the "long felt need" traversal:

> First, the need must have been a persistent one that was recognized by those of ordinary skill in the art...Second, the long-felt need must not have been satisfied by another before the invention by applicant...
>
> Third, the invention must in fact satisfy the long-felt need.

40. None of these factors are met by the mere reliance upon the dates and ages of the references cited. It is also stated in MPEP 716.04 II that "Long-felt need is analyzed as of the date the problem is identified and articulated, and there is evidence of efforts to solve that problem, not as of the date of the most pertinent prior art references." From this, it is clear that Applicant's argument that the age of the references demonstrates a "long felt need" is incorrect.

There is no statement or other clear articulation that the problem was known in 1995, the earliest priority date of Mennemeier, nor was there a statement identifying the problem in Chehrazi. There is also no evidence that there were efforts to solve the problem. This must all be proven and the evidence supporting the proof must be provided via a 37 CFR 1.132 Affidavit before the "long felt need" traversal will be considered.

41. Applicant's argue in essence on pages 12-13

> ...There is no indication in the claim that they [a media processor and a central processing unit (CPU)] are the same processor...
>
> Therefore, the rejection...is based on the improper interpretation of the claim...

42. This has not been found persuasive. The claim language explicitly recites in claim 23 "wherein the microprocessor is a media processor disposed on an integrated circuit with a memory controller" and in claim 41 "a central processing unit (CPU)". A media processor inherently has a CPU to execute the instructions being run on the media processor. Claim 41 does not contain any language suggesting that the CPU being referred to in the claim is a ***separate*** CPU from that in the media processor. Claim 41 only states "***a*** central processing unit (CPU)" which includes the CPU in the media processor itself in the scope of the claim. There is no language stating that the CPU being referred to in claim 41 is separate and different from the CPU found in the media processor. Therefore, the claim language in claim 41 is unclear as to which CPU is being referred to, i.e. the CPU on the media processor or a separate CPU. When claim 41 is read with the interpretation that the CPU is the media processor's CPU, then it is unclear how the media processor's CPU is both on and off the integrated circuit. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is

noted that the features upon which applicant relies (i.e., a central processing unit separate from the central processing unit in the media processor) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

43. Applicant's argues in essence on page 14 "It is impermissible to simply make a hindsight reconstruction of the claimed invention using the claim as a template and filling the gaps using the elements from the references." This has not been found persuasive. In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

44. Applicant argues in essence on pages 14-15 and 17-18 "If the reasoning of the Office Action were followed, microprocessors, buses and remote palm top computers would be all memory controllers..." This has not been found persuasive. The reasoning in the Office Action were not that microprocessors, buses and remote palm top computers were all memory controllers. The reasoning was that memory controllers were an inherent feature found in these devices, whether they were explicitly taught in a reference or not. A memory controller, in the broadest reasonable interpretation of the term, is a device that controls memory accesses. In order for instruction to be retrieved and the data for the instructions to be retrieved and saved to

memory, there is a device arbitrating the memory accesses in these situations. Without the arbitrator, memory would randomly be broadcasting data and randomly be written to, thereby corrupting execution and data. Chehrazi has taught in the lines cited in the rejection above that there is memory, e.g. RAM, ROM, and main memory, that is accessed. Whether the memory controller is a separate unit, as Applicant seems to be arguing, or a side function of the media processor, it does not matter. Each functions similarly in that it controls accesses, e.g. reads and writes, to the memory of the device. There must be a memory controller in the system for these memories to be accessed properly, as is shown in Watkins et al., "A Memory Controller with an Integrated Graphics Processor" ©1993; Petrick et al., U.S. Patent Number 5,892,966; and Hennessy and Patterson's Computer Architecture: A Quantitative Approach ©1996 page 73.

45. Applicant argues in essence on page 18 "...the Office Action misapplied the elements of Chehrazi, based on the description about the MADD instruction...which is clearly not the SABD instruction and/or based on speculation in view of..." This has not been found persuasive. The system is applicable to "operands of various data types." This includes floating point operations and, to conclude, that floating-point operations are applicable only for one instruction in a media processor based upon its exemplary description is incorrect. Also, Chehrazi in column 9, lines 23-26 states that the result is a "256-bit result" which is floating-point data. In addition, media processors normally operate on both integer and floating-point data.

Conclusion

46. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure

a. Kitagaki et al., U.S. Patent Number 5,450,553, has taught the details of the selection method, e.g. selecting the positive result after subtracting the two operands from each other, when executing an absolute difference operation.

b. Uratani et al., U.S. Patent Number 5,610,850, has taught the details of the selection method, e.g. selecting the positive result after subtracting the two operands from each other, when executing an absolute difference operation.

c. Petrick et al., U.S. Patent Number 5,892,966, has taught a media processor with a memory controller and using Sun's Visual Instruction Set, which includes a single floating-point absolute difference instruction with a destination storage register.

d. Yung, U.S. Patent Number 5,996,066, has taught a graphics processor with a memory controller on a single integrated circuit.

e. Hirairi, U.S. Patent Number 6,028,987, has taught the details of the selection method, e.g. selecting the positive result after subtracting the two operands from each other, when executing an absolute difference operation.

f. Watkins et al.'s "A Memory Controller with an Integrated Graphics Processor" ©1993 has taught a graphics processor with memory controller on a single integrated circuit.

g. Sun's "Visual Instructions set (VIS™) User's Guide" ©1997 has taught a single absolute difference instruction for floating-point numbers with a destination storage register.

47. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

48. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

49. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:00am-4:30pm.

50. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

51. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL

Aimee J. Li
9 January 2006

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100